

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance, TrenchPLUS current sensing and diodes for ESD protection.

Product availability:

BUK7109-75AIE in SOT426 (D<sup>2</sup>-PAK)

BUK7909-75AIE in SOT263B (TO-220AB).

### 1.2 Features

- Integrated current sensor
- ESD protection
- Q101 compliant
- Standard level compatible.

### 1.3 Applications

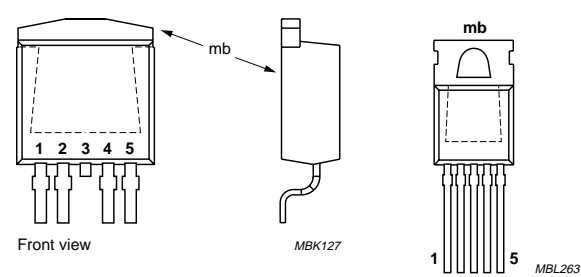
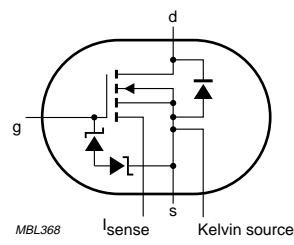
- Variable Valve Timing for engines
- Electrical Power Assisted Steering.

### 1.4 Quick reference data

- $V_{DS} \leq 75$  V
- $I_D \leq 120$  A
- $R_{DSon} = 8.0$  m $\Omega$  (typ)
- $I_D/I_{sense} = 500$  (typ).

## 2. Pinning information

Table 1: Pinning - SOT426 and SOT263B, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	$I_{sense}$		
3	drain (d)		
4	Kelvin source		
5	source (s)		
mb	mounting base; connected to drain (d)	<p style="text-align: center;">SOT426 (D<sup>2</sup>-PAK)                      SOT263B (TO-220AB)</p>	

### 3. Limiting values

**Table 2: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)		-	75	V
$V_{DGS}$	drain-gate voltage (DC)		-	75	V
$V_{GS}$	gate-source voltage (DC)		-	±20	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2 and 3	[1] -	120	A
			[2] -	75	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2	[2] -	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	480	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	272	W
$I_{GS(CL)}$	gate-source clamping current	continuous	-	10	mA
		$t_p = 5\text{ ms}; \delta = 0.01$	-	50	mA
$T_{stg}$	storage temperature		-55	+175	°C
$T_j$	junction temperature		-55	+175	°C
<b>Source-drain diode</b>					
$I_{DR}$	reverse drain current (DC)	$T_{mb} = 25\text{ °C}$	[1] -	120	A
			[2] -	75	A
$I_{DRM}$	peak reverse drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	480	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 75\text{ A};$ $V_{DS} \leq 75\text{ V}; V_{GS} = 10\text{ V};$ $R_{GS} = 50\text{ }\Omega;$ starting $T_j = 25\text{ °C}$	-	739	mJ
<b>Electrostatic discharge</b>					
$V_{esd}$	electrostatic discharge voltage; all pins	Human Body Model; $C = 100\text{ pF};$ $R = 1.5\text{ k}\Omega$	-	6	kV

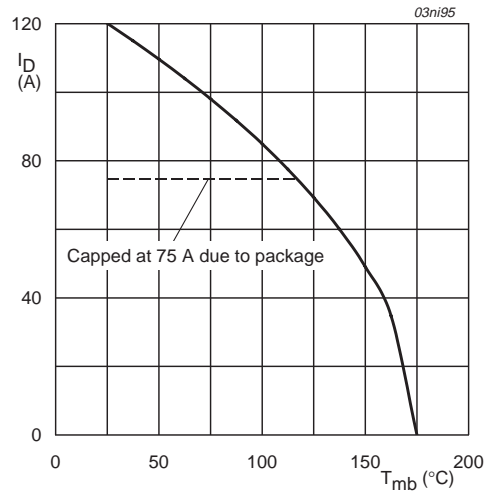
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package.



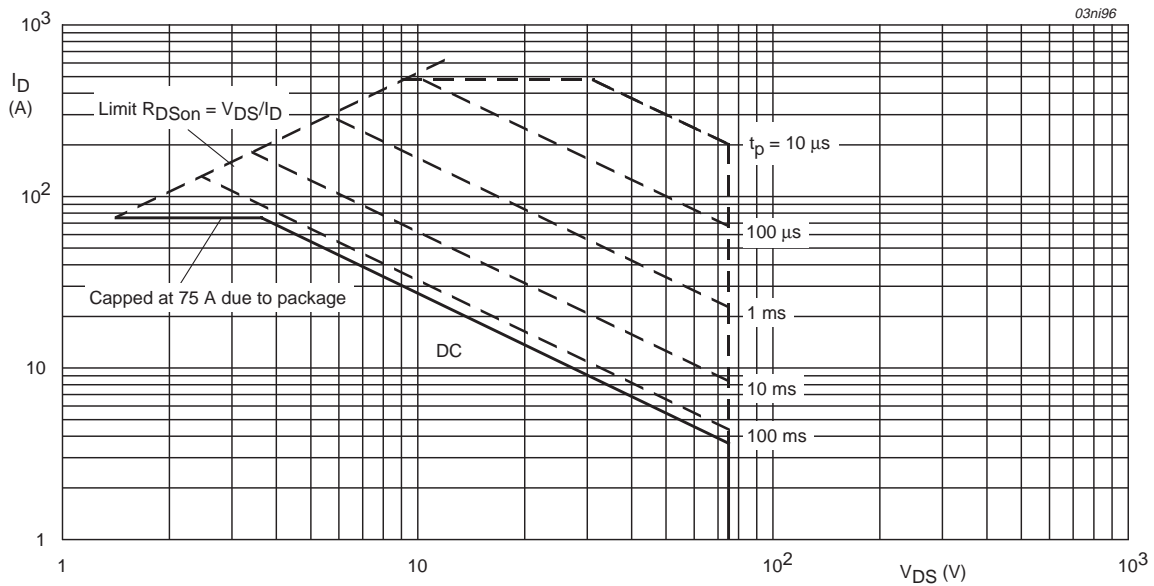
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10\text{ V}$

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

### 4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT263B	vertical in still air	-	60	-	K/W
	SOT426	minimum footprint; mounted on a PCB	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.55	K/W

#### 4.1 Transient thermal impedance

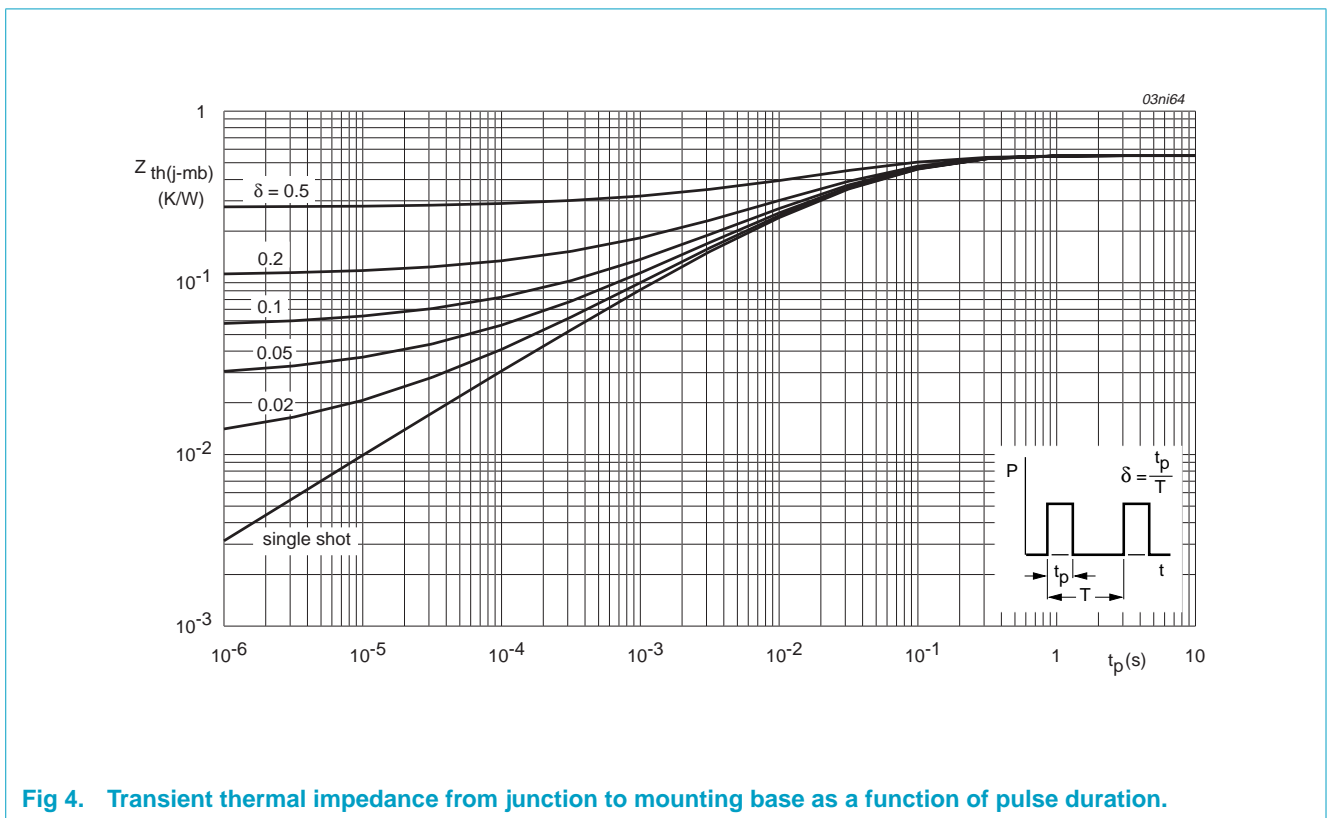


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 5. Characteristics

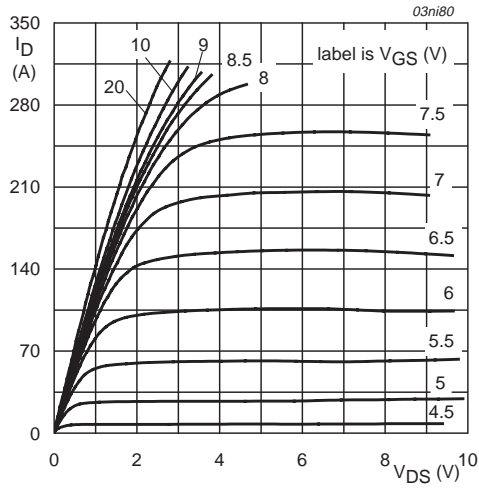
**Table 4: Characteristics**
 $T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	75	-	-	V
		$T_j = -55\text{ °C}$	70	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ <b>Figure 9</b>				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 175\text{ °C}$	1	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 75\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.1	10	$\mu\text{A}$
		$T_j = 175\text{ °C}$	-	-	250	$\mu\text{A}$
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = \pm 1\text{ mA};$ $-55\text{ °C} < T_j < 175\text{ °C}$	20	22	-	V
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	22	1000	nA
		$T_j = 175\text{ °C}$	-	-	10	$\mu\text{A}$
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 50\text{ A};$ <b>Figure 7 and 8</b>				
		$T_j = 25\text{ °C}$	-	8	9	m $\Omega$
		$T_j = 175\text{ °C}$	-	-	19	m $\Omega$
$I_D/I_{sense}$	ratio of drain current to sense current	$V_{GS} > 10\text{ V};$ $-55\text{ °C} < T_j < 175\text{ °C}$	450	500	550	
<b>Dynamic characteristics</b>						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 10\text{ V}; V_{DS} = 60\text{ V};$ $I_D = 25\text{ A};$ <b>Figure 14</b>	-	121	-	nC
$Q_{gs}$	gate-source charge		-	20	-	nC
$Q_{gd}$	gate-drain (Miller) charge		-	44	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$ $f = 1\text{ MHz};$ <b>Figure 12</b>	-	4700	-	pF
$C_{oss}$	output capacitance		-	800	-	pF
$C_{rss}$	reverse transfer capacitance		-	455	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega;$ $V_{GS} = 10\text{ V}; R_G = 10\text{ }\Omega$	-	35	-	nS
$t_r$	rise time		-	108	-	nS
$t_{d(off)}$	turn-off delay time		-	185	-	nS
$t_f$	fall time		-	100	-	nS
$L_d$	internal drain inductance	measured from upper edge of drain mounting base to centre of die	-	2.5	-	nH
$L_s$	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH

### Source-drain diode

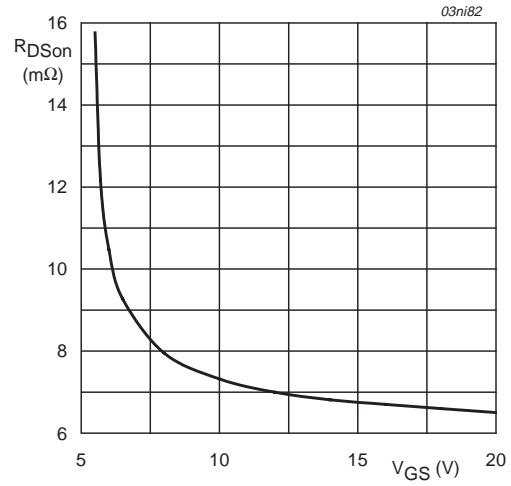
**Table 4: Characteristics...continued***T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; Figure 16	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs	-	75	-	ns
Q <sub>r</sub>	recovered charge	V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 30 V	-	270	-	nC



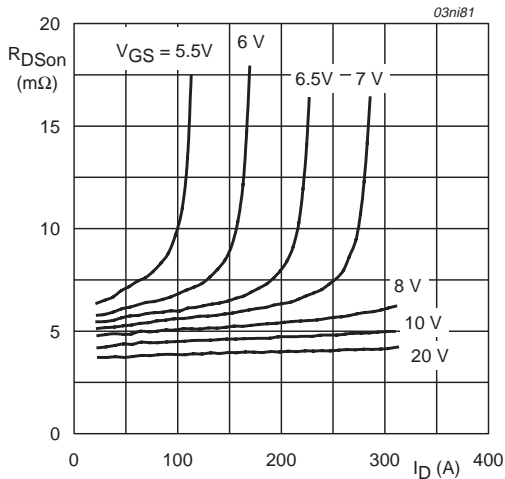
$T_j = 25\text{ }^\circ\text{C}$ ;  $t_p = 300\text{ }\mu\text{s}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



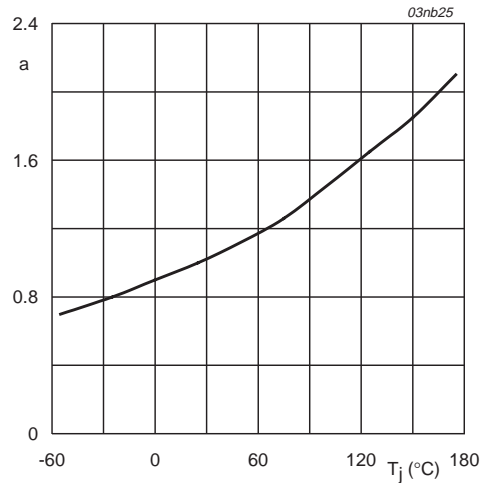
$T_j = 25\text{ }^\circ\text{C}$ ;  $I_D = 50\text{ A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.**



$T_j = 25\text{ }^\circ\text{C}$ ;  $t_p = 300\text{ }\mu\text{s}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



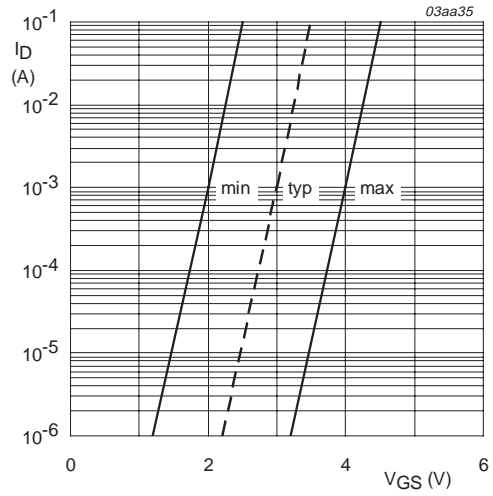
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



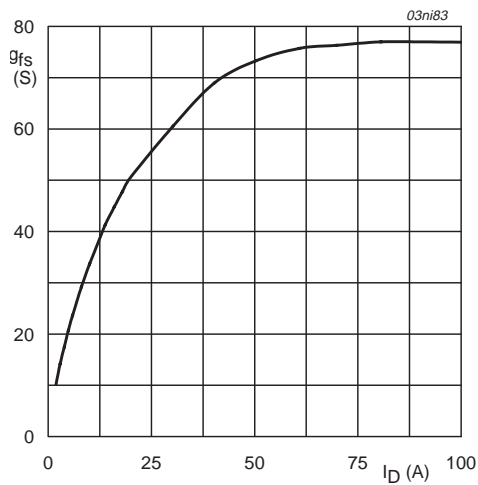
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



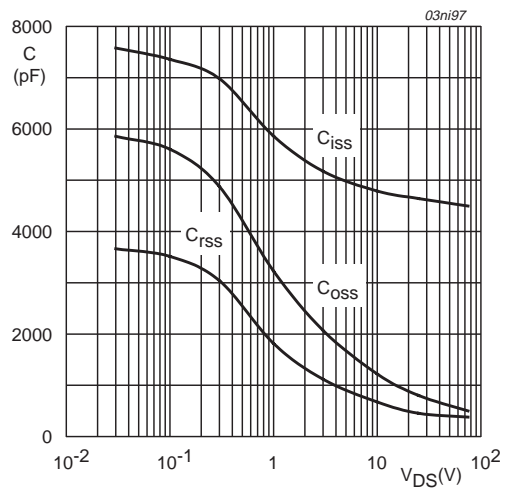
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

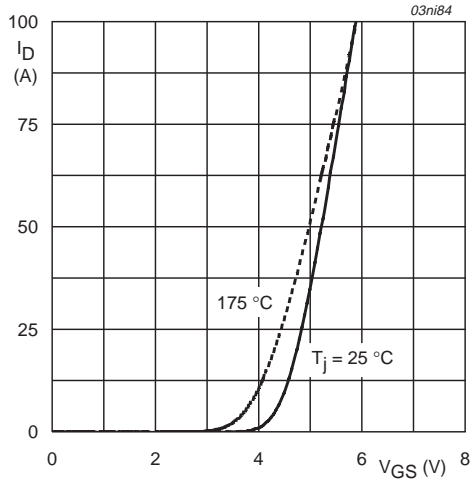
**Fig 11. Forward transconductance as a function of drain current; typical values.**



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

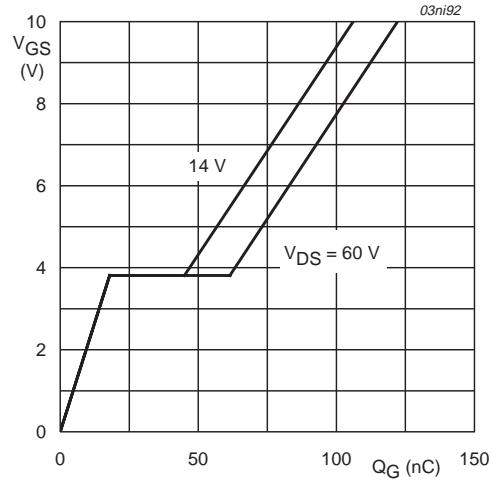
**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**





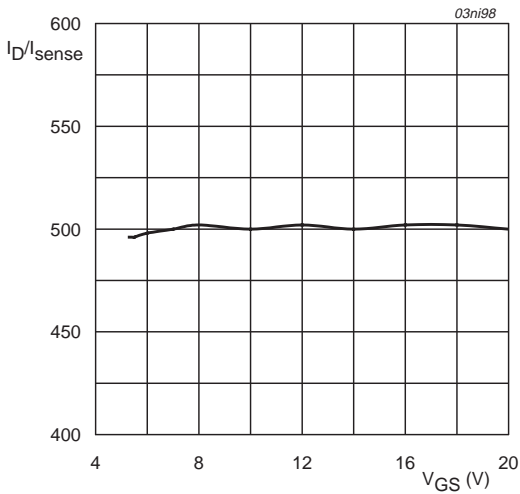
$V_{DS} = 25 \text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



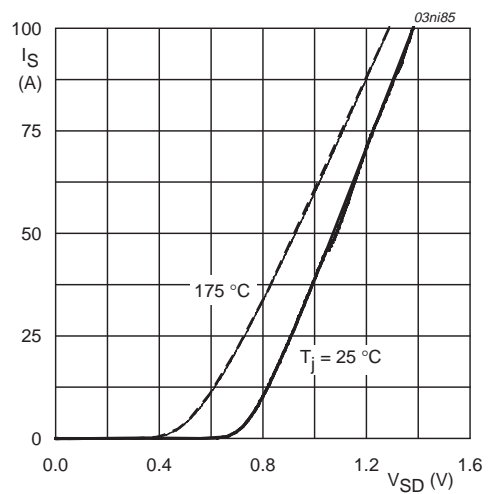
$T_j = 25 \text{ }^\circ\text{C}; I_D = 25 \text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



$I_D = 25 \text{ A}$

Fig 15. Drain-sense current ratio as a function of gate-source voltage; typical values.



$V_{GS} = 0 \text{ V}$

Fig 16. Reverse diode current as function of reverse diode voltage; typical values.

6. Package outline

Plastic single-ended surface mounted package (Philips version of D<sup>2</sup>-PAK); 5 leads (one lead cropped)

SOT426

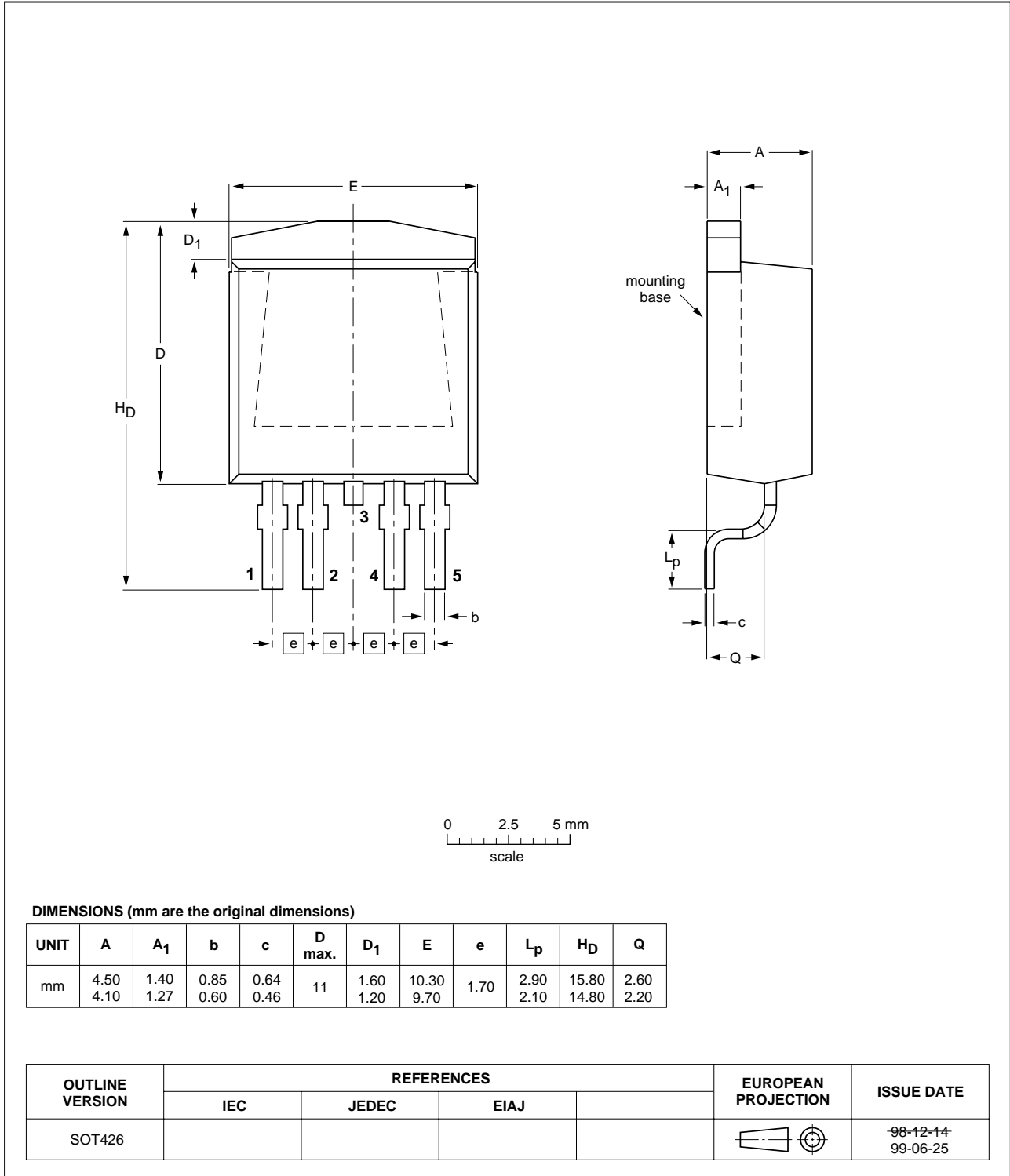


Fig 17. SOT426 (D<sup>2</sup>-PAK).

Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220

SOT263B

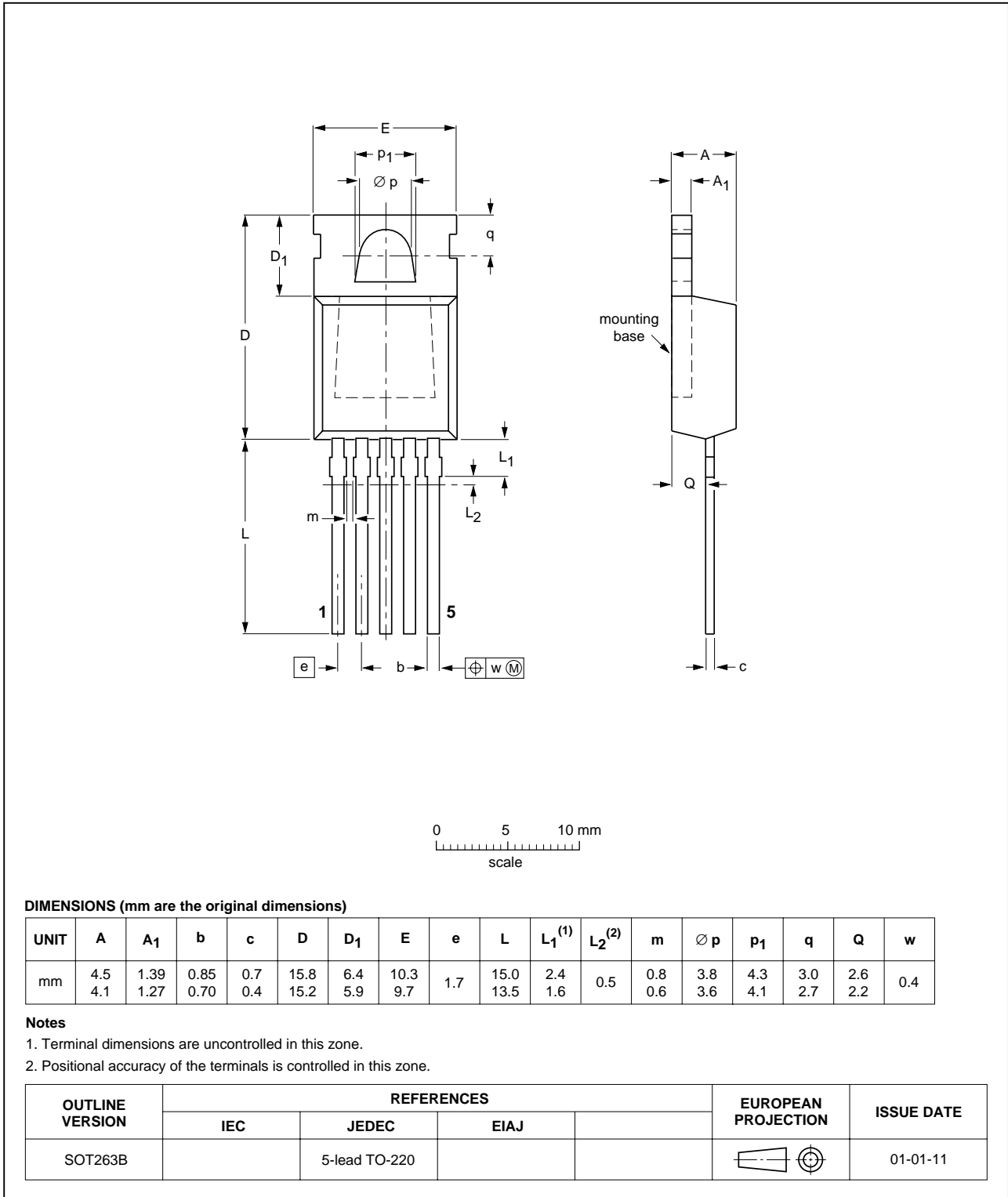
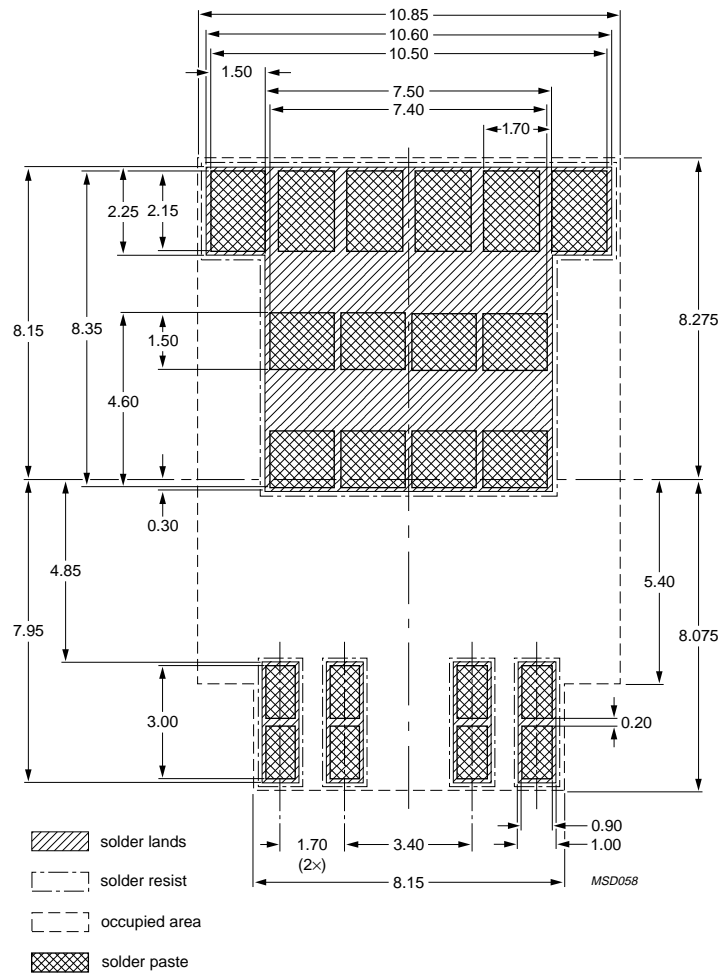


Fig 18. SOT263B (TO-220AB).

## 7. Soldering



Dimensions in mm.

Fig 19. Reflow soldering footprint for SOT426.

## 8. Revision history

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Table 5: Revision history

Rev	Date	CPCN	Description
01	20020809	-	Product data; initial version

## 9. Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## Contents

<b>1</b>	<b>Product profile</b> .....	<b>1</b>
1.1	Description .....	1
1.2	Features .....	1
1.3	Applications .....	1
1.4	Quick reference data .....	1
<b>2</b>	<b>Pinning information</b> .....	<b>1</b>
<b>3</b>	<b>Limiting values</b> .....	<b>2</b>
<b>4</b>	<b>Thermal characteristics</b> .....	<b>4</b>
4.1	Transient thermal impedance .....	4
<b>5</b>	<b>Characteristics</b> .....	<b>5</b>
<b>6</b>	<b>Package outline</b> .....	<b>10</b>
<b>7</b>	<b>Soldering</b> .....	<b>12</b>
<b>8</b>	<b>Revision history</b> .....	<b>13</b>
<b>9</b>	<b>Data sheet status</b> .....	<b>14</b>
<b>10</b>	<b>Definitions</b> .....	<b>14</b>
<b>11</b>	<b>Disclaimers</b> .....	<b>14</b>
<b>12</b>	<b>Trademarks</b> .....	<b>14</b>

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